UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,993	09/25/2003	Francesco Pappalardo	851763.439	4505

500 7590 06/01/2007

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 5400
SEATTLE, WA 98104

EXAMINER	
ODOM, CURTIS B	
ART UNIT	**PAPER NUMBER**
2611	

MAIL DATE	DELIVERY MODE
06/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,993	PAPPALARDO ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) *28-36,39,51 and 52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27, 37, 38, and 40-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 37 and 38 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims recite a computer program not encoded on a computer readable medium. MPEP 2106.01 [R-5], Section I states the following:

> **Similarly, computer programs claimed as computer listings per se, i.e., the descriptions or expressions of the programs, are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. See Lowry, 32 F.3d at 1583-84, 32 USPQ2d at 1035. Accordingly, it is important to distinguish claims that define descriptive material per se from claims that define statutory inventions.**

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 8-12, 15, 21-25, 40-42, 44-46, 49, and 50 are rejected under 35 U.S.C. 102(b) as being anticipated by Devanney et al. (U. S. Patent No. 6, 243, 779).

Regarding claim 1, Devanney et al. discloses a process for transmitting at given instants digital signals on a bus (see column 4, lines 44-51), the digital signals being transmitted on the bus selectively in a non-encoded format and in an encoded (inverted) format (see column 5, lines 1-5 and 63-64), comprising comparing a signal to be transmitted on the bus for an instant of the given instants with a signal transmitted on the bus for a preceding instant among the given instants using a bit-wise comparison circuit as described in column 7, lines 10-48) so as to minimize switching activity on the bus by reducing the switching noise (see Abstract), wherein the operation of comparing is carried out bit by bit (see column 7, lines 10-48) in orderly sequence so as to identify in the context of the signal to be transmitted on the bus at an instant of the given instants and of the signal transmitted on the bus for the preceding instant among the given instants, a first set of bits that are not changed during normal transmission (see column 5, lines 1-5) and a second set of bits (next data word) that are changed by inversion (see column 5, lines 53-64); and a decision whether to transmit the signals on the bus in non-encoded format and in encoded format is taken limitedly to the bits of the second set of bits by using a bit-wise inverter circuit (see Fig. 6, column 9, line 50-column 6, line 8) which either transmits bits in a non-encoded format or an encoded (inverted) format depending on a control signal (INVERT) for each bit.

Regarding claim 8, Devanney et al. discloses transmitting bits of the first data word (set of bits) in a non-encoded (non-inverted) format on the bus (see column 5, lines 1-5).

Regarding claim 9, Devanney et al. discloses encoding (inverting) bits on the bus if the comparison reveals that any bit (which includes a first bit) in the sequence differs (is changed), see column 9, lines 44-49).

Regarding claim 10, Devanney et al. discloses always transmitting bits of the first data word (set of bits) in a non-encoded (non-inverted) format on the bus (see column 5, lines 1-5).

Regarding claim 11, Devanney et al. discloses the encoded format is obtained by inverting bits of the signal in non-encoded format (see column 5, lines 52-64).

Regarding claim 12, Devanney et al. discloses associating with the digital signals an additional indicator signal (see column 5, lines 17-30) that is able to assume, at the given instants, different logic values (0 or 1) according to whether the digital signal to which it is associated is transmitted in the non-encoded format (see column 5, lines 17-30) and, at least in part, in the encoded format, respectively, so that the additional signal is able to modify a logic value between successive instants of the given instants rather than modifying the entire signal (see column 5, lines 23-30);

detecting, for the digital signals, occurrence of a condition in which transmission on the bus in the non-encoded format and in the encoded format are able to give rise to an identical switching activity on the bus by comparing bits of a present data word and a next data word (see column 5, lines 40-60); and

deciding whether the signal to be transmitted on the bus at a given instant is to be transmitted in the non-encoded format or in the at least partially encoded format (see column 5, lines 53-64) so as to cause the additional indicator signal associated with the signal to be transmitted on the bus at a given instant to keep the logic value at 1 for a third data word (see

column 5, lines 32-39) with respect to the logic value assumed by the additional signal associated with the signal (second data word) transmitted on the bus for the preceding instant among the given instants (see column 5, lines 23-30).

Regarding claim 15, Devanney et al. discloses an encoder (see Fig. 1, sending circuit) for transmitting at given instants on a bus digital signals selectively in a non-encoded format (see column 5, lines 1-5) and an encoded (inverted) format (see column 5, lines 53-64), the encoder comprising:

a comparison module (see Fig. 4, block 210, column 7, lines 10-48) for comparing a signal to be transmitted on the bus for an instant of the given instants (next data word) with a signal transmitted on the bus for the preceding instant (present data word) among the given instants, and generating at least one corresponding decision signal (BIT_MISMATCH); and

a transmission-driving module (as described in column 4, lines 44-48) for driving transmission of the signals on the bus in non-encoded format and in encoded (inverted) format according to the decision signal (see column 8, lines 21-31) so as to minimize a switching activity (noise) on the bus (as described in the Abstract),

wherein the comparison module comprises a logic network that is able to compare bit by bit, in orderly sequence (see column 7, lines 10-48), the signal (next data word) to be transmitted on the bus at an instant of the given instants and the signal (present data word) transmitted on the bus for the preceding instant among the given instants, so as to identify a first set of bits (present word) that are not changed and a second set of bits (next word) at least some of which are changed (see column 5, lines 53-64); and

the transmission-driving module is configured for driving the transmission of the signals on the bus in non-encoded format and in encoded format limitedly to the bits of the second set of bits by using a bit-wise inverter circuit (see Fig. 6, column 9, line 50-column 6, line 8) which either transmits bits in a non-encoded format or an encoded (inverted) format depending on a control signal (INVERT) for each bit.

Regarding claim 21, Devanney et al. discloses driving transmission of a first bit on the signal to be transmitted on the bus in a non-encoded (non-inverted) format (see column 5, lines 1-5).

Regarding claim 22, Devanney et al. discloses encoding (inverting) bits on the bus if the comparison (logic network) reveals that any bit (which includes a first bit) in the sequence differs (is changed), see column 9, lines 44-49).

Regarding claim 23, Devanney et al. discloses always driving transmission of a first set of bits to be transmitted on the bus in a non-encoded (non-inverted) format (see column 5, lines 1-5).

Regarding claim 24, Devanney et al. discloses an inverter circuit for generating the encoded format (see Fig. 6, column 9, line 50-column 6, line 8).

Regarding claim 25, Devanney et al. discloses a module for associating with the digital signals an additional indicator signal (see column 5, lines 17-30) that is able to assume, at the given instants, different logic values (0 or 1) according to whether the digital signal to which it is associated is transmitted in the non-encoded format (see column 5, lines 17-30) and, at least in part, in the encoded format, respectively, so that the additional signal is able to modify a logic

value between successive instants of the given instants rather than modifying the entire signal (see column 5, lines 23-30);

a module for detecting, for the digital signals, occurrence of a condition in which transmission on the bus in the non-encoded format and in the encoded format are able to give rise to an identical switching activity on the bus by comparing bits of a present data word and a next data word (see column 5, lines 40-60); and driving signals to be transmitted on the bus (see column 5, lines 1-5) at a given instant to be transmitted in the non-encoded format or in the at least partially encoded format (see column 5, lines 53-64) so as to cause the additional indicator signal associated with the signal to be transmitted on the bus at a given instant to keep the logic value at 1 for a third data word (see column 5, lines 32-39) with respect to the logic value assumed by the additional signal associated with the signal (second data word) transmitted on the bus for the preceding instant among the given instants (see column 5, lines 23-30).

Regarding claim 40, Devanney et al. discloses a method of encoding a digital signal, comprising:

transmitting a first signal represented by a present data word (see column 5, lines 1-5);

comparing a second signal (next data word) to the first signal (see column 5, lines 53-64 and column 6, lines 18-28);

identifying a first set of bits (see column 5, lines 53-64 and column 6, lines 18-28) in the second signal that are not changed and a second set of bits in the second signal at least some of which are changed based on the comparison to the first signal;

processing the first set of bits in a first manner by not encoding the bits (see column 5, lines 1-5);

processing the second set of bits in a second manner by inverting the bits (see column 5, lines 53-64); and

transmitting the processed first and second sets of bits (see column 5, lines 1-5).

Regarding claim 41, Devanney et al. discloses transmitting the first signal on a bus (see column 4, line 66-column 5, line 5).

Regarding claim 42, Devanney et al. discloses wherein comparing the second signal to the first signal comprises sequentially comparing bits of the second signal with corresponding bits of the first signal (see column 7, lines 10-48) until the comparison does not yield a match (BIT_MISMATCH) and the first set of bits comprises the bits that yielded a match, wherein if each bit of the first signal and second signal match, then the first signal would comprise of bits which yielded a match.

Regarding claim 44, Devanney et al. discloses transmitting the first set of bits (see column 5, lines 1-5) in a non-encoded format and the second set of bits in an encoded (inverted) format (see column 5, lines 53-64).

Regarding claims 45 and 46, Devanney et al. discloses encoding the first and second set of bits using a bus-inverter encoding process (see column 6, line 50-column 10, line 8).

Regarding claim 49, Devanney et al. discloses a bit-wise inverter (see Fig. 6) for transmitting bits of the second set of bits in either an encoded (inverted) or non-encoded format depending a control signal (INVERT) for each bit.

Regarding claim 50, Devanney et al. discloses generating a control signal (INVERT) based on the comparison (see column 9, lines 4-30) and transmitting the control signal to the bus (see column 9, lines 29-30).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3-7, 16-20, 37, 38, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devanney et al. (U. S. Patent No. 6, 243, 779).

Regarding claims 3-7, 16-20, and 43, Devanney et al. discloses the comparison by the logic network is a bit-by-bit comparison of the all the bits in the signals (see column 7, lines 10-48), wherein an INVERT signal may be generated for any number of bits which differ (see column 9, lines 43-48). Devanney et al. does not specifically disclose the comparison starts from a bit with a least probability of change, a most significant bit, a least significant bit, exploring other bits subjected to comparison moving in a given direction, or exploring other bits subject to comparison moving in opposite directions. However, it would have been obvious to one skilled in the art at the time the invention was made that since Devanny et al. discloses comparing all the bits, the starting point of the of the comparison in the sequence is variable and differing the starting point in the comparison would not change the functionality of Devanney et al. since in the end, all the bits will be compared. Thus, based on the above disclosure, claims 3-7, 16-20, and 43 are rejected as being obvious over Devanney et al.

Regarding claims 37 and 38, Devanney et al. discloses all the limitations of claims 37 (see rejection of claim 1) and 38 (see rejection of claim 15) except the method/apparatus implemented as software. However, it would have been obvious to one skilled in the art at the time the invention was made to implement the method/apparatus of Devanney et al. as software to perform the same function of the hardware for less expense, greater adaptability, and greater flexibility. Thus, claims 37 and 38 are rejected as being obvious over Devanney et al.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Devanney et al. (U. S. Patent No. 6, 243, 779) in view of Grivna (U. S. Patent No. 6, 539, 051).

Regarding claim 2, Devanney et al. does not disclose a marker bit that separates the bits of the first set (present data word) for the bits the of the second set (next data word).

However, Grivna discloses frame marker bits to bound or separate data according to a pre-defined framing sequence or pattern (see column 7, lines 26-41). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the transmission of Devanney et al. with the frame marker bits of Grivna since Grivna discloses the marker bits allow proper extraction of transmitted data characters (bits), see column 7, lines 26-41.

8. Claims 13, 14, 26, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devanney et al. (U. S. Patent No. 6, 243, 779) in view of Lin et al. (US 2002/0133777).

Regarding claims 13, 14, 26, and 27, Devanney et al. does not disclose determining a Hamming distance between the first set of bits and the second set of bits.

However, Lin et al. discloses determining a Hamming distance between a first set of non-encoded bits and a second set of encoded bits (see section 0035). Therefore, it would have been

obvious to one skilled in the art to determine the Hamming distance between the sets of bits in Devanney et al. as disclosed by Lin et al. since Lin et al. states determining and reducing the Hamming distance will not result in transmission errors (see section 0036).

9. Claims 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devanney et al. (U. S. Patent No. 6, 243, 779) in view of Blaum et al. (U. S. Patent No. 5, 280, 533).

Regarding claims 47 and 48, Devanney et al. does not disclose the first or second set of bit is an empty set. However, Blaum et al. discloses a coding technique including two sets of bits, wherein one set is an empty set, wherein the sets of bits are compared (see column 3, lines 12-30). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to include an empty set of bits in Devanney et al. as disclosed by Blaum et al. since Blaum et al. states the coding technique corrects received transitions (bits), see column 3, lines 36-45.

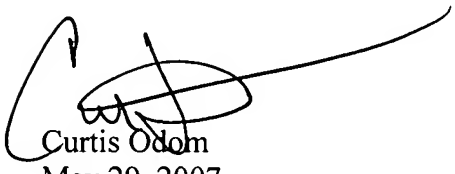
Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kamishima (U. S. Patent No. 6, 008, 744) discloses comparing the MSB of bit sequences are inverting bits based on the comparison.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Curtis Odom
May 29, 2007